

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF

Confirmation No.: 2032

ASAI et al.

Group Art Unit: 2841

Appln. No.: 09/529,597

Examiner: H. Bui

Filed: May 31, 2000

Title: PACKAGE SUBSTRATE

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TECHNOLOGY CENTER 2800#19/ Amitt D
R. 312 (att)Declaration
R. Tyson
3/4/02

February 13, 2002

AMENDMENT UNDER 37 C.F.R. § 1.312Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Responsive to the Notice of Allowability mailed January 14, 2002 and the telephone conferences of February 7 and February 13, 2002, and prior to issuance, please amend the patent application identified above as follows:

IN THE SPECIFICATION:

Please amend the paragraph extending from page 6, line 26 to page 7, line 11 as follows:

In a package board according to a first aspect of the invention, the soldering pads on the IC chip side surface of the package board are small, so the rate of the metallic portion occupied by those soldering pads is also small. On the other hand, the soldering pads on the mother board side surface of the package board are large, so the rate of the metallic portion occupied by those soldering pads is also large. This is why a dummy pattern is formed between conductor circuit patterns on the IC chip side surface of the package board thereby to